

Introduction of IC Manufacturing to Amateurs

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Abstract: In the fabrication of silicon wafers to create integrated circuits, chemistry and physics play a significant role. It is important to change the silicon wafer surface conditions and properties using both innocuous and harmful compounds, particular and uncommon circumstances, plasma-state elements, and RF (Radio Frequency) energies. Starting with the production of silicon wafers, sands are molten under high temperature in order to change its molecular structure. In this process, silicon ingot with particular diameter is formed and sliced into pieces of wafer. Following by chemical manufacture, wafer would be prepared to be fabricated into integrated circuits. Then, the circuits would be drawn onto the wafer through oxidation, photolithography, etching, diffusion, and ion implanlation. After those fabrication, all these components (transistors, resistors, capacitors, and so on) were only accessible as discrete units, would have taken up most of a medium-sized room 20 years ago, the devices currently fill a one-inch square IC's surface. When it comes to wafer sorting, a systematic mode will be used to take each bad die from the whole die pie. The researchers will use the relative finder and tester to gain the situation for each die and this work will bring foundation to the following stages including packaging and final test. The packaging process comes to the next consideration. This work divides the packaging process into five steps. All those steps are listed clearly in the essay below, from sawing up the wafer into an individual die to marking the packages. The final process after packaging is the final test. The final test is not such complicated. So this work only introduces the devices that it will use and its purpose.

1. Introduction

1.1 Chips of silicon

In the first stage of wafer manufacturing process, a large perfect silicon crystal is formed. There is a 'seed crystal' that is a perfect crystal and would grow into the required size with sufficient supply of molten granular powder as the silicon source. Then the seed is immersed gradually into the crucible containing the molten powder and drawn out slowly ^[1-4].

1.2 The basic manufacture of IC

This fabrication process manufactures the silicon wafer into integrated circuit under extremely clean condition. Engineering, metallurgy, chemistry, and physics are all involved in the painstaking, meticulous process of turning silicon into memory chips. The "wires" and "components" are drawn onto the wafer by special techniques ^[5-7].

1.3 The wafer testing

Followed by the testing process, which is mainly to distinguish the bad dies from the whole plates, which will use the probe card and series of equipment including the automatic tester and the finder to check out whether the problems really occur or not ^[8, 9].

1.4 The covering stage

The manufacture of semiconductor devices for use in electronic devices ends with integrated circuit packaging. The semiconductor material block is protected from physical harm and corrosion by an encapsulating casing. The electrical contacts that connect the gadget to a circuit board are supported by the case, also referred to as a "package."

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Fig. 1: Normal Outlook of IC after being packaged
(<https://www.wellpcb.com/ic-packaging.html>)

Ceramic flat packs, which were employed by the military for a long time because of their dependability and compact size, were an early form of integrated circuit packaging. The ICP (Integrated Circuit Package), a ceramic package with the leads on one side and aligned with the package axis, was the other type of packaging utilized in the 1970s. However, the commercial circuit packaging preferred DIP (dual in-line package). And the raw material changed from ceramic to plastic. In the 1980s VLSI (very large-scale integration) pin counts exceeded the practical limit for DIP packaging which leads to PGA (pin grid array) and LCC (leadless chip carrier) packages. Surface mount packaging appeared in the early 1980s and became popular in the late 1980s. Area array was the next innovation of packaging. In the late 1990s, PQFP (plastic quad flat pack) and TSOP (thin small-outline packages) replaced PGA packages as the most common for high pin count devices (Figure 1).

Due to the complexity of packaging, there are several considerations during the production, such as electrical, mechanical, and thermal and economic problems. Scientists are working on them and trying to figure them out to improve the standard of packaging process.

1.5 Eventual test

During the packaging process, the die is prone to sustain damage. Therefore, it may not function properly in part. In order to ensure that no ICs that have been improperly

packaged are transported, the final test must be conducted on every packaged IC. It can classify the material into various performance groups in addition to determining whether or not it is properly packaged. The most expensive parts are those with the highest speed grades since they are the scarcest and best performing. Why does the discrepancy exist? It is mostly caused by process differences that happen during wafer processing and across wafers as well as wafer to wafer.

2. The process of manufacturing

2.1 Silicon wafer

Obtaining the sand An extremely pure and high-quality form of silicon must be present in the sand used to grow the wafers. Because of this, not just any sand collected from the beach will do. The majority of the sand supplied for these operations comes from Australian beaches (figure 2).

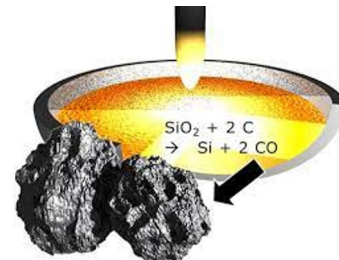


Fig. 2: Crucible [2]

Preparing the molten silicon bath Just beyond its melting point, at a temperature of around 1600 degrees, the sand (SiO_2) is placed in a crucible. The silicon that will make up the wafer will come from the molten sand.

Making the ingot The molten silicon bath is now filled with a pristine silicon seed crystal. As it rotates, this crystal will be gently removed. The Czochralski (cz) method is the most often used method. The outcome is an ingot, which is a cylindrical piece of pure silicon (figure 3).

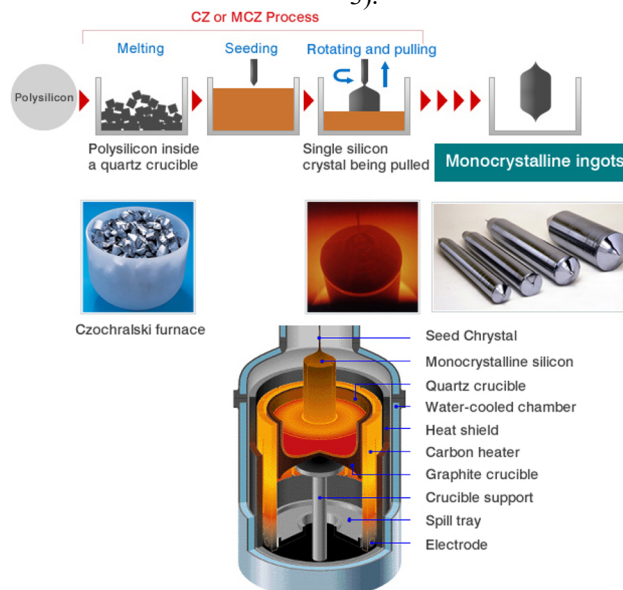


Fig. 3 Stages of making ignots [2]

The purpose of this procedure is to prepare a thoroughly clean surface for processing later. If a layer of silicon is chemically produced on top of the wafer, it is of far higher quality than the layer of silicon that is already present in the wafer but is only marginally damaged or filthy. The procedure will actually take place on the epitaxial layer. The temperature factors as well as the rate at which the silicon ingot is removed determine the diameter of the silicon ingot. The ingot is withdrawn after it is the proper length, after which it is ground to a consistent external surface and diameter. Each wafer has either a notch or a flat edge that will be utilized to position the wafer later.

Slice the wafers The ingot is sliced into the required piece of wafers by a diamond saw once it has been ground into set diameter. Next, the wafers would be polished until the surfaces achieve the standard of smooth and thickness

2.2 Wafer fabrication

Cleaning These fabrication processes, transforming the silicon into integrated circuits, require the circumstance of none contaminants. Therefore, the chambers of fabrication are usually maintained under vacuum. The chambers manipulate all types of contaminants strictly.

Oxidation The ability of silicon to oxidize is one of the key factors in its widespread use as a semiconductor material. It enables silicon to develop a top-notch insulating layer on a wafer. Silicon reacts with oxygen to generate silicon dioxide, which is what glass is made of, when silicon is exposed to oxygen or water vapor at a high temperature. The layer functions as an excellent barrier and insulator and is stable even in high temperature conditions (figure 4).

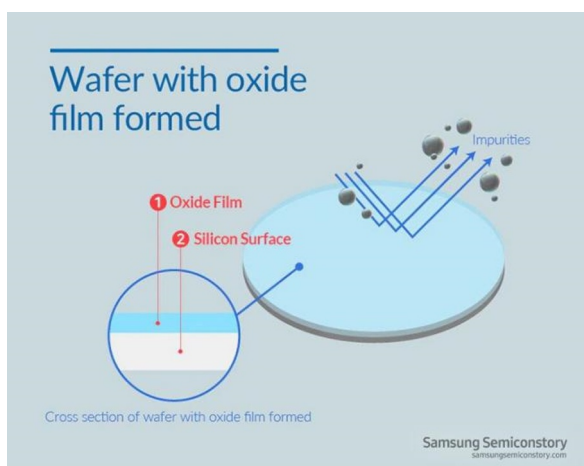


Fig. 4 Light-sensitive cover^[2]

Photolithography The wafer is then uniformly covered in a thick liquid known as photoresist, which is light-sensitive. While the wafer is rotating, the coating is applied. By precisely positioning a mask between the wafer and an ultraviolet light source, sections of the wafer are chosen for exposure. Light penetrates the transparent parts of the mask and reveals the photoresist there (figure 5).

In this technique, the mask is much further away from the wafer, and the image is transferred to the wafer via a

series of lenses. The key benefit of this technique is the much larger mask than the final pattern and that the photoresist can be exposed under a better resolution by optical and mechanical manipulations. At the moment, this approach is the most popular one in business. When exposed to UV light, photoresist becomes harder and etchants cannot penetrate it. Due to this chemical alteration, the exposed, hardened photoresist can remain on the wafer while the unexposed photoresist can be removed by the developer solution.

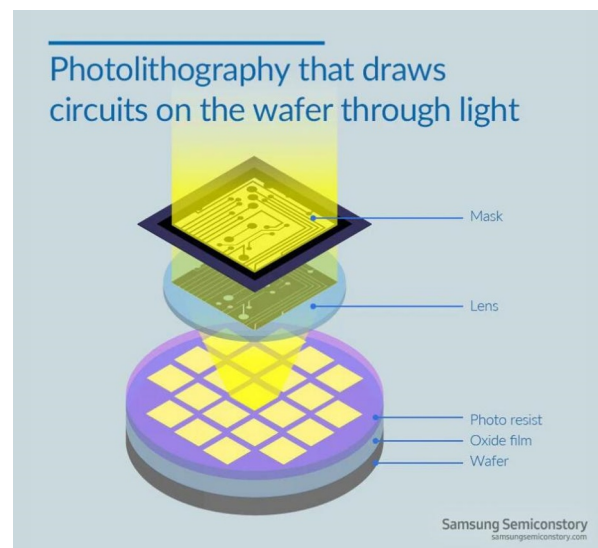


Fig. 5 Schematic graph of photobiography^[2]

Etching The undesirable material is removed from the wafer immediately following photolithography using the etching technique. Due to the lack of selection in this technique, photoresist has to be used to trace the design onto the wafer. Wet etching and dry etching are the two primary etching techniques. This leaves a wafer pattern that is identical to the mask's design. Then, using a different chemical, the hardened photoresist is eliminated.

Methods of Etching:

- Wet Etching
- Dry Etching
- Plasma Etching
- Reactive Ion Etching
- Ion Milling

Anisotropic Etching vs. Isotropic Etching

Diffusion In a furnace, wafers are subjected to diffusion as a gas flow passes over them. This phase must come before the photoresist and patterning because, like the etch, it is not selective. Imagine oxidation to better comprehend the operations of this step. With the exception of employing a gas other than oxygen, diffusion and oxidation are highly comparable processes.

Ion implantation Ion implantation differs from diffusion. In contrast to diffusion, which leverages the natural condition of gas to travel where there is no gas, ion implantation injects the desired dopant ions into the wafer. The greatest comparison for ion implantation is to shooting a machine gun against a wall. In this comparison, the wafer represents the wall, while the ions represent the bullets. Ion implantation's primary drawback is that technique can only process one wafer at a time, whereas a diffusion chamber can process multiple wafers.

Drive In

This is the subsequent stage after the ions have been injected into the wafer. The magnets used to regulate the ion beam. The wafer is heated in this step to encourage the ions to penetrate it more deeply.

Annealing

An additional stage of heating is necessary due to the enormous harm that these processes—especially ion implantation—can bring to the wafer. The wafer is heated during this last step so that its crystal lattice structure can self-heal. A complex sandwich of n- and p-type silicon, as well as insulating layers of glass and silicon nitride, makes up the completed wafer. During the initial mask procedures, all three circuit components (transistor, resistor, and capacitor) are built. The following steps integrate these circuit elements. The surface is covered by a layer of glass (called BPSG) as insulator and a contact mask is utilized to determine the contact points or windows. Then the whole wafer is covered by a thin layer of aluminum in a sputtering chamber when the contact windows have been etched.

The next step involves connecting the various circuit elements using a contact mask. An insulating layer known as BPSG is then deposited to define the contact points. After the windows are etched, the entire process is carried out in a sputtering chamber. The aluminum layer is then covered with a fine network of wires and thin metal connections.

2.3 Wafer sorting

Each die manufactured has a great amount of cushions called bond pads on which it is going to be attached to the

chip during the process. The mold is coated with a layer to protect, except for in which the liner is. As for every die which are going to be tested, there are "probe cards" with a series of needles spaced apart from each other so that they queued with bond pad openings (figure 6).

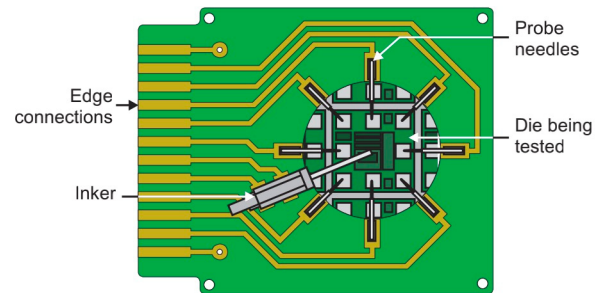


Fig. 6 The distribution of the wafer finder ^[3]

The wafer under test is fixed to a disk in a device called a wafer finder. The probe also takes the probe card, placing the probe card needle on the bond pad on the die, touches the needle down to make the electrical connection for the test, and then lifts the needle and places it on the next die after the test.

The wafer finder is connected to a tester, which is an automatic device that does electrical tests on each one die. The electronic testing tool is generally a computing device and a number of power supplies, gauges and function generators that can be programmed to perform various electronic measurements. The tester communicates with the probe to tell when each die is being tested and whether the die is up to scratch, and when the die fails, a small ink point might be applied to the die to record it, or an entry will be made into the map to indicate the position of the worse chips (figure 7).

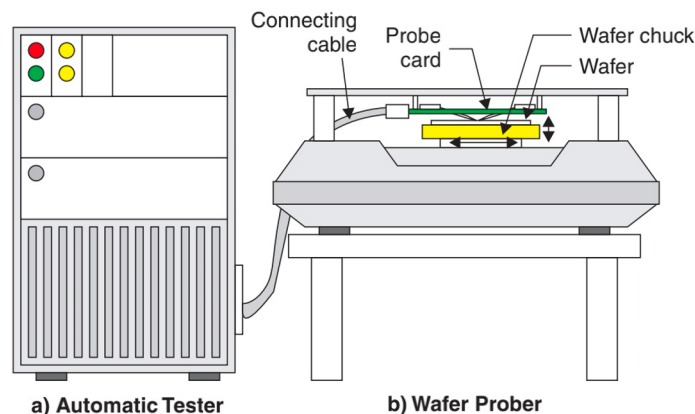


Fig. 7 The graph of the automatic tester and wafer prober ^[3]

2.4 Packaging

Saw up the wafer into the individual die The wafer is affixed onto adhesive tape that is stretched across a metal frame following the wafer test. The wafer has adhered to the tape from its reverse, or non-circuit side. The die is split apart using an automated high-speed saw with a very thin diamond blade. To prevent sawing from harming the IC circuitry, there is a roadway between each die that is devoid of electronics. The individual die is held in place after sawing by the sticky tape.

Mount the die into the leadframe Now, each working die on the wafer is taken off the sticky tape and put on a lead frame, which is a metal frame. Automated pick-and-place devices carry out this procedure. The pattern for the electrical connection pins that protrude from the packaging are etched or stamped onto the lead frame. The die is epoxy fixed to a pad that is part of the lead frame as well (figure 8).

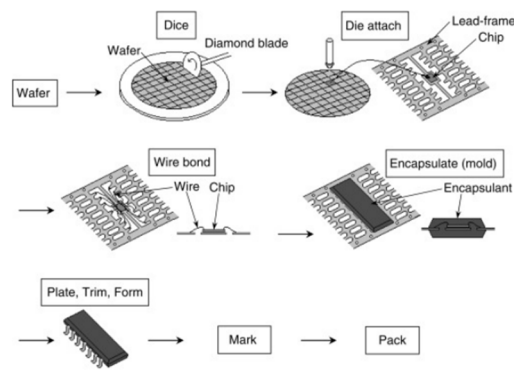


Fig. 8 Flowchart of the IC packaging^[6]

Wirebond from the die bond-pads to the leadframe

Now, each bond pad is connected by a little wire, usually made of gold, to a corresponding lead frame pin. These are the electrical links that connect the die to the pins, and ultimately to the outside world. Additionally, automated machines referred to as wire bonders can execute wire bonding (figure 9).

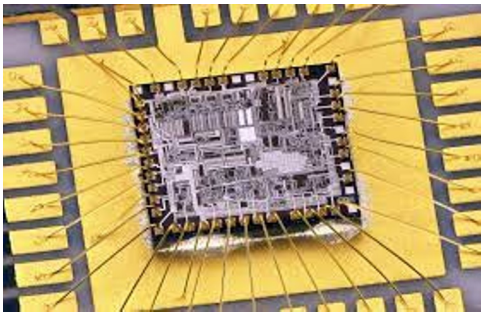


Fig. 9 Wire bonders^[7]

Mold epoxy around the die to protect it The lead frame pins are now protruding from a rectangular patch of black epoxy that has been formed around the die and lead frame. Large presses with heat and pressure are used for molding.

Trim and form to break the individual ICs apart A mechanical tool now punches out each packaged IC from the lead frame bars that held the units in rows. The tool also bends the leads forming them into their final configuration.

Mark the packages The units are branded with a part number, company name, date, etc. on the epoxy plastic to identify the part.(4) (figure 10)

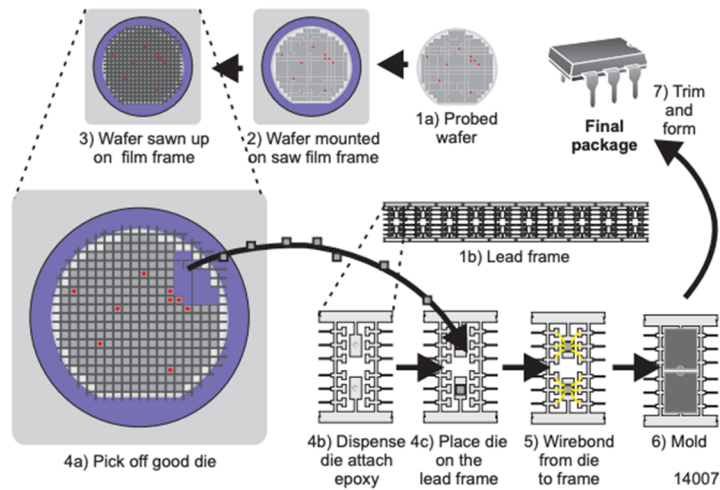


Fig. 10 Specific Processes of Packaging^[4]

2.5 Final Test

The final test is comparable to the wafer test, with the exception that connections are made and the IC packages are "handled" by a handler. It is based on comparing the values of each pin's voltage, current, and resistance (figure 11).

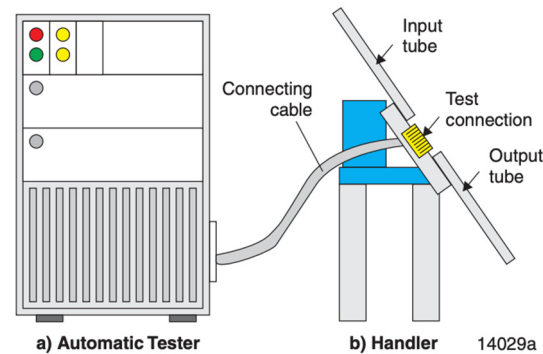


Fig. 11 The Outlook of the Tester^[4]

The handler is attached to a tester that is comparable to or exact to the wafer test tester. Defective units are now discarded, while the working ones are prepared for shipping.

*Tester- a computer controlled system that performs electrical tests automatically.^[4]

Handler- a piece of equipment that moves parts from an input bin, makes electrical connection to the parts for testing, and then moves the parts to a output bin or bins. Operates under control of the tester

3. Outlook

According to the statement above, we found that the main improvement can mainly be used in the wafer sorting and packaging, because in reality, the easy and direct way to reduce the cost is through these two parts.

3.1 The improvement in wafer sorting

A test strategy to balance the test cost and the cost of undetected yield fallout is needed to bring heterogeneous integration to high-volume production. Thanks to innovations in MEMS probe card technology, customers can mix-and-match between full test coverage KGD test flow (such as FormFactor's Altius probe card that supports 45µm grid-array pitch microbump probing for at-speed HBM and interposer validation) and high-throughput test flow with acceptable risk for limited test^[9, 10]

3.2 The enhancement in packaging

Electrical The materials used as electrical contacts exhibit characteristics like low resistance, low capacitance, and low inductance. Both the structure and materials must prioritize signal transmission properties while minimizing any parasitic elements that could negatively affect the signal.

Mechanical and thermal The materials of the package are either plastic (thermoset or thermoplastic), metal (commonly Kovar), or ceramic. A common plastic used for this is epoxy-cresol-novolak (ECN). All three forms of material provide useful heat, moisture, and mechanical strength. However, metallic and ceramic packages are frequently favoured for more expensive devices because of their greater robustness (which also permits larger pin-count designs), heat dissipation, hermetic performance, or other factors.

For those dehiscences, the most efficient way to solve that is to choose the proper epoxy and use an ultrasonic scanner to check the quality of the products which can notice even nanometer-scale dehiscences.

4. Conclusion

The main idea for all these complex steps of wafer fabrication should be chasing the efficiency and the lower cost, there will be absolutely users and producers asking and suspecting the bad quality and the high cost of these

process, but after hundreds of thousands of tries and improvement, hopefully there will be some results that give us a sense of satisfaction.

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